CURRENT SOURCE

FIELD OF THE INVENTION

[0001] The present invention relates generally to current sources and, in particular, to current sources having extended voltage range.

BACKGROUND

[0002] Constant current sources provide suitable supplies of bias current to analog circuit blocks, including amplifiers and comparators. Interface circuits use comparators to distinguish between logical voltage levels, definitions for which range from SSTL-3 to SSTL-2 and SSTL-1.8. Operation of these interfaces generally assumes a bias voltage at midlevel between ground (VSSQ) and supply (VDDQ). Over the years, the bias voltage of Integrated Circuits (ICs) has dropped from 5V to 1.25V and in the future can be expected to drop to 0.9V. Nevertheless, the threshold voltage for the ICs has remained constant at about .5V, leaving very little swing room between the bias voltage and the threshold voltage in which the transistor can produce constant current. At current biasing levels, a device can quickly leave its saturation region and enter its linear region. As the device enters its linear region, the amplification of the amplifier or comparator is degraded.

[0003] Although a bias voltage at mid-level presents symmetry to the driving circuits of the interface, it also creates a severe challenge for receiver circuits regarding the required voltage (e.g., common-mode) range. For example, achieving an operating range at a reference voltage of 1.25V, with a signal swing of +/- 310mV in an SSTL-2 interface, is difficult. This is true even if designers use NFET technology having low threshold voltages. Achieving an operating range at a reference voltage of 0.9V with an allowable signal swing of +/- 250mV in an SSTL-1.8 interface is even more difficult. To address this problem, a wide operating range and NFETS having low threshold voltages are desirable. For example, an existing approach is shown in Figure 1a, which depicts one of many ways to design a constant current source driving a differential stage. The gate voltage VIREF controls a current source transistor 102. The drain of transistor 102 is connected to the common source of the differential pair of transistors 104 and 106, which in the illustrated embodiment are NFET and, particularly N-MOS, transistors. Nodes CLK and bCLK, in this example, are fully differential input signals to transistors 104 and 106, respectively. Node 108 follows the lower of the input nodes less a

threshold voltage. As the voltage at node 108 decreases, it drives transistor 102 out of saturation, thereby reducing the current through transistor 102. Reducing the current flow in transistor 102 causes an increase in the transition delay of the differential stage. This presents a problem, because it is desirable to keep delay constant. However, in this circuit, any change in the current would modulate the delay time. Equally problematic are fluctuations in the current which result in modulating the delay in a differential amplifier.

[0004] Extending the operating range of a current source eliminates the need for more complex and expensive solutions, such as adding costly negative supply voltages to extend the voltage range. An unmet need exists for a circuit that can extend the voltage range of a current supply in a simple and inexpensive manner. Furthermore, to avoid changes in current source levels over a wide voltage range, an unmet need exists to provide a current source and gate drive apparatus capable of providing a constant current when the current source transistor is biased in either the saturated or linear regions of operation.

SUMMARY OF THE INVENTION

[0005] The present invention contemplates the extension of a voltage range of a current source, where a gate voltage of a current source transistor is regulated based on the transistor's drain voltage. An embodiment of the present invention accordingly can provide a constant current source even when a current source transistor exits its saturation region.

[0006] An embodiment of one aspect of the present invention is directed towards extending the voltage range of a current supply in an IC where the drains of two transistors are connected to each other and a third current source driving transistor has its gate connected to the drains of the two transistors. Further, the drain of the third transistor is connected to the sources of the first two transistors.

[0007] In another embodiment, a device is connected to the drain of either the first or second transistor. This device could be a fully differential receiver circuit, a single ended receiver circuit, a differential amplifier circuit, or any other possible circuit that could be connected to an embodiment of the present invention.

[0008] In another embodiment of the present invention, a power source is connected to the positive terminal of a current source. The negative terminal of the current source is connected to the drains of two transistors. A third current source driving transistor has its gate connected to the drains of the two transistors. Furthermore, the drain of the third transistor is connected to the sources of the first two transistors.

[0009] Another embodiment of the present invention provides a method for extending a voltage range of a current source in an IC, in which the drains of two transistors are connected to each other. The sources of those first two transistors are connected to each other, and the drain of a third current source driving transistor is connected to the sources of the first two transistors. Further, the gate of the third transistor is connected to the drains of the first two transistors.

[0010] In another embodiment of the present invention, a circuit is provided for extending a current source's voltage range. The circuit comprises a means for regulating a gate to source voltage using a differential pair and a means for driving current by using a current driving transistor.

[0011] According to a further embodiment of the present invention, a current source for use in an integrated circuit to provide an extended voltage range comprises a circuit for measuring a drain voltage using a differential pair, and a circuit for regulating a gate voltage based on the drain voltage measured at the differential pair.

[0012] In another embodiment of the present invention, a method for extending a voltage range of a current source in an integrated circuit provides a constant current source in the saturation region of a transistor and maintains that constant current even when the transistor exits the saturation region.

[0013] In another embodiment of the present invention, a method for extending a voltage range of a current source in an integrated circuit is provided in which a drain voltage of a transistor is measured and a gate voltage is regulated based on the drain voltage of that transistor.

[0014] In another embodiment of the present invention, a method for extending a voltage range of a current source in an integrated circuit is provided which measures a drain voltage using a differential pair and regulates a gate voltage based on the drain voltage measured at the differential pair.

[0015] Yet another embodiment of the present invention is a method for extending a voltage range of a current source in an integrated circuit. The method comprises the steps of providing a first transistor and a second transistor, the first transistor having a drain terminal and the second transistor having a gate terminal, measuring the drain terminal voltage of the first transistor, and based on the drain terminal voltage, regulating the gate terminal voltage of the second transistor.

[0016] Another embodiment of the present invention is a current source for use in an integrated circuit having an extended voltage range comprising a transistor having a drain characterized by a voltage. In this embodiment, a gate has a voltage that is reactive to the voltage of the drain.

BRIEF DESCRIPTION OF DRAWINGS

[0017] Figure 1a is a diagram of a conventional differential amplifier.

[0018] Figure 1b is a diagram showing an embodiment of a circuit according to the present invention.

[0019] Figure 2a shows the relationship between drain voltage and gate voltage in a transistor delivering constant current in an embodiment of a circuit according to the present invention.

[0020] Figure 2b shows the relationship between the drain voltage and drain current of a current source transistor utilizing an embodiment of the present invention and a conventional current source circuit.

[0021] Figure 3a shows a conventional differential amplifier used as a receiver.

[0022] Figure 3b is a diagram showing an embodiment of a circuit according to the present invention.

[0023] Figure 3c shows a differential amplifier using a prior art current source.

[0024] Figure 4 shows simulation results of receiver delay using a differential input signal in an embodiment of a circuit according to the present invention in comparison with simulation results of receiver delay using a conventional input circuit.

[0025] Figure 5 shows a comparison similar to that of Figure 4, but using different values for the circuit components.

DETAILED DESCRIPTION

[0026] Figure 1b illustrates an embodiment of a control circuit according to the present invention, based on the receiver circuit of Figure 1a, and including feedback as further described below. The circuit shown in Figure 1b generates a VIREF used in a circuit according to the present invention shown in Figure 3b, as will be described below. In Figure 1b, power supply 202 is connected to current source 204, which may be an on-chip band gap regulator or other suitable current source. Transistors 206 and 208, which in the illustrated embodiment are NMOS transistors, form a differential pair, the drains of transistors 206 and 208 being connected to each other, as well as to current source 204. In an aspect of the present invention, transistors 206 and 208, have equal width-to-length (W/L) ratios. In the illustrated embodiment, but without limitation, transistors 206 and 208 have W/L ratios of 4 to 0.4. Depending upon the requirements of a specific application, the W/L ratio may be suitably varied.

[0027] According to an aspect of the present invention, and in contrast to the conventional circuit of Figure 1a where the voltage seen by transistor 102 is constant, the gate of NMOS current driving transistor 210 is connected to the drains of transistors 206 and 208 at node 212, enabling the voltage at the gate of current driving transistor 210 to be regulated by the drains of transistors 206 and 208. In an aspect of the present invention, transistor 210 has a W/L ratio of 55 to 0.45. The W/L ratio may be suitably varied depending upon the requirements of a specific application. As further discussed below, in the circuit of Figure 1b the current through transistor 210 will remain constant even as transistor 210 leaves the saturation region.

[0028] The voltage at node 214 follows the lower of the input voltages at transistors 206 and 208, less a threshold voltage of 0.5 volts or lower, resulting in a reduced drain voltage at transistor 210. With CLK and bCLK signals driving the gates of transistors 206 and 208, respectively, a drain voltage is developed on node 214. A resulting gate voltage on transistor 210 allows transistor 210 to conduct at the current level dictated by current source 204, regardless of its drain voltage. In contrast to the conventional circuit of Figure 1a, in which the lower of CLK and bCLK can be sufficiently low to drive transistor 102 out of saturation and reduce performance of the differential pair of transistors 104 and 106, the current reference level output by current source 204 of the circuit according to the present invention will accordingly flow through transistor device 210 independent of whether transistor 210 is in saturated or linear mode. The gate

voltage on 210 adjusts to insure that the reference current of current source 204 will be maintained as the voltage of CLK and bCLK is adjusted.

[0029] The response time of a circuit to changes in current flow through the circuit is an important design consideration. The response time of the circuit according to the present invention, as illustrated, can be adjusted by connecting capacitor 216 to node 212. When capacitor 216 has low capacitance, the voltage at node 212 and the gate of transistor 210 will change quickly in response to changes of inputs CLK and bCLK. A low capacitance at 216 may lead to a rapidly varying signal at the gate of transistor 210. On the other hand, when the capacitance of capacitor 216 is high, the voltage at node 212 and gate 210 would have a greater tendency to remain stable during transitions. Therefore, node 212 and the gate at 210 would not reach the correct voltage until the capacitor had charged, leading, in turn, to circuit delay. The value of the capacitance, therefore, is selected to meet the constraints of the resulting circuit's application, taking into account both the character of typical input waveforms and the desired response characteristics.

[0030] Figures 2a and 2b together show the operation of the circuit of Figure 1b. As illustrated in Figure 2a, a decreasing drain voltage on transistor 210 causes the gate voltage on 210 to increase. Figure 2b shows the relationship between the drain current and drain voltage of transistor 210 and that, with this improved source, the current stays constant even as the drain voltage varies. With a decreasing drain voltage, as in Figure 2a, the gate voltage Vgs (gate to source) increases. Figure 2b also shows how an increase in the gate voltage Vgs will increase the current through transistor 210. At higher Vgs, a desired current can be sustained at smaller drain voltages. The current therefore remains constant, even when the device leaves saturation and enters the linear region, in which the current flow would normally begin to decrease.

[0031] Figure 3a shows a conventional differential receiver. Voltage source 300 is connected to transistors 302 and 306, which in the illustrated embodiment are PMOS transistors. Transistors 302 and 306 may have W/L ratios which are equal, according to an aspect of the invention, and that are set according to the design constraints of their specific intended application. In one embodiment, but without limitation, they have W/L ratios of 8 to 0.5. The gates of transistors 302 and 306 are also connected to the drain of transistor 306 to create a current mirror. This current mirror forces the amount of current flowing through transistors 302 and 306 to be equal. Transistor 312, which in

the illustrated embodiment is an NMOS transistor, acts as a current source for the current mirror and has a gate connected to VIREF.

[0032] In conventional circuits, such as in Figure 3a, the gate of current source transistor 312 or its equivalent is connected to a stable voltage that maintains the source-drain current at a desired level, so long as transistor 312 remains biased in the saturated region. As lower-voltage technologies are developed, the DC operating points of differential amplifiers are diminishing to the point where it is difficult to maintain a current source that is coupled to a differential pair biased in its saturated region. For example, in a 1V technology with 200mv threshold voltages, an input reference level of 0.5V will be typically used. To maintain conduction of differential devices such as transistors 104 and 106 in Figure 1a, and analogous transistors described with reference to the embodiments in Figures 1b and 3a-3c, their source nodes are preferably 0.5V-0.2V=0.3V. This requires that the drain voltage of the current source be at 0.3V. At drain voltages lower than 0.3V on current source transistor 312, the current begins to fall off as transistor 312 enters the linear range of operation. This drop in current will result in undesirable changes to propagation delay through the differential amplifier.

[0033] Referring to Figure 3b, the structure in Figure 3a has been adapted to provide a constant current source for a typical differential amplifier in an embodiment of an aspect of the present invention. This occurs by coupling the circuit shown in Figure 1b to the VIREF shown in Figure 3a at node 212. In Figure 3b, a constant current source level 204 has been derived from an on-chip bandgap reference or by other convenient methods and is used to supply a reference current into differential pair of transistors 206 and 208. With CLK and bCLK signals driving the gates of transistors 206 and 208 respectively, a drain voltage is developed on node 214. A gate voltage on device 210 will result which will allow device 210
to conduct at the current level dictated by current reference 204, regardless of the drain voltage of device 210. The current reference level output by 204 will flow through device 210 independent of whether device 210 is in saturated or linear mode, and the gate voltage on 210 will adjust to insure the reference current will flow as the voltage of CLK and bCLK is adjusted.

[0034] The voltage level on the gate of device 210, VIREF, is used to gate the current source transistor 312 in the differential amplifier formed by transistors 104, 106, 306 and 302. The matching of the W/L ratios between transistors 104,106 and 302,306, are important in determining the amount of current flow through the circuit. As inputs CLK and bCLK swing around a voltage point, the VIREF level will be adjusted by the inventive structure to maintain a constant current in current source transistor 312. Using the improved current source described above, propagation delay through the differential amplifier is held more constant, and particularly as the voltage drops, current is maintained and propagation delay time does not increase.

[0035] As shown in Figure 3c, a prior art current source can be connected to input VIREF. Nevertheless, as will be shown, the delay of this circuit is greater and less predictable than the delay that results from the circuit in Figure 3b.

[0036] Figure 4 shows the simulation results of receiver delay for a differential input signal from a circuit according to the present invention in comparison with a circuit according to the prior art. The lower curve of Figure 4 represents the receiver delay for the embodiment of a circuit according to the present invention of Figure 3b. The control voltage 212 is connected to the gate of current source transistor 312 such that constant current will be supplied to differential transistors 104 and 106. The circuit in Figure 3b sustains the same current flow even when current source transistor 312 exits the saturation region. This is because the gate voltage of transistor 312 in Figure 3b is connected to node 212 which, as stated earlier, increases in voltage as the drain voltage of the current driving transistor decreases. Thus, even when the voltage at the drain of transistor 312 decreases, the gate voltage of transistor 312 will increase to compensate by action of the control circuit according to Figure 1b. The upper curve of Figure 4 represents the receiver delay for the circuit in Figure 3c. Figure 3c has a prior art configuration for a current source. Figure 4 demonstrates that compared to a conventional prior art current source, the current driving transistor 312 which is connected to an embodiment of a circuit according to the present invention has a signal whose receiver delay is diminished and more constant over a wider voltage range.

[0037] In the example of Figure 4, capacitor 216 has a capacitance of zero. Figure 5 is an analysis of the same circuit as in Figure 4 and illustrates the same comparison of delay between Figures 3b and 3c, but uses a capacitor value of 1pF for capacitor 216.

[0038] The current source according to the present invention is useful in single- ended IC applications. Referring to the embodiment shown in Figure 1b, for example, a single-ended application is created when the gate terminals of transistors 206 and 208 are tied to node 212. In a single-ended system, a lower capacitance on capacitor 216 is recommended for improved symmetry between rising and falling edges.

[0039] This technique has been demonstrated using NFET current sources and differential pairs for purposes of illustration, but any suitable transistors could be used. For example, various embodiments of the circuits and methods according to the present invention can be created wherein PFET current sources and, or PFET differential pairs are used.

[0040] While the invention has been particularly shown and described with reference to particular embodiments, those skilled in the art will understand that various changes in form and details may be made without departing form the spirit and scope of the invention as set forth in the appended claims.